RNA51953A, B

Voltage Detecting, System Resetting IC Series

REJ03D0911-0402
Rev.4.02
Apr 01, 2010

Description

RNA51953A,B are semiconductor integrated circuits designed for detecting supply voltage and resetting all types of logic circuits such as CPUs.

They include a built-in delay circuit to provide the desired retardation time simply by adding an external capacitor.

They fined extensive applications, including battery checking circuit, level detecting circuit and waveform shaping circuit.

Features

- Few external parts
- Large delay time with a capacitor of small capacitance (td ≈ 100 ms, at 0.33 μF)
- Low threshold operating voltage (Supply voltage to keep low-state at low supply voltage):
  0.6 V (Typ) at RL = 22 kΩ
- Wide supply voltage range: 2 V to 17 V
- Wide application range
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)	Surface Treatment
RNA51953AFPH0	SOP-8 pin	PRSP0008DE-C	FP	H (2,500 pcs / Reel)	0 (Ni/Pd/Au)
RNA51953APT0	DIP-8 pin	PRDP0008AF-B	P	T (1,000 pcs / Reel)	0 (Ni/Pd/Au)
RNA51953BFPH0	SOP-8 pin	PRSP0008DE-C	FP	H (2,500 pcs / Reel)	0 (Ni/Pd/Au)
RNA51953BPT0	DIP-8 pin	PRDP0008AF-B	P	T (1,000 pcs / Reel)	0 (Ni/Pd/Au)

Application

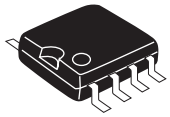
- Reset circuit of Pch, Nch, CMOS, microcomputer, CPU and MCU, Reset of logic circuit, Battery check circuit, switching circuit back-up voltage, level detecting circuit, waveform shaping circuit, delay waveform generating circuit, DC/DC converter, over voltage protection circuit

Recommended Operating Condition

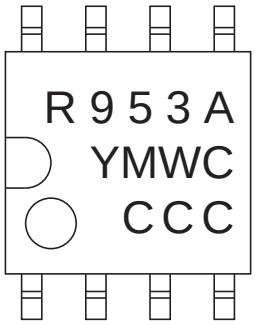
- Supply voltage range: 2 V to 17 V

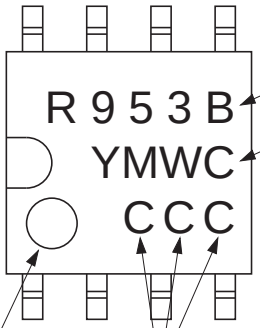
Outline and Article Indication

• RNA51953A, B

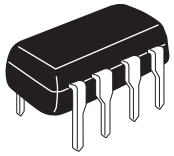


SOP-8

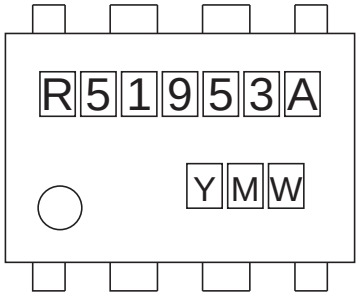


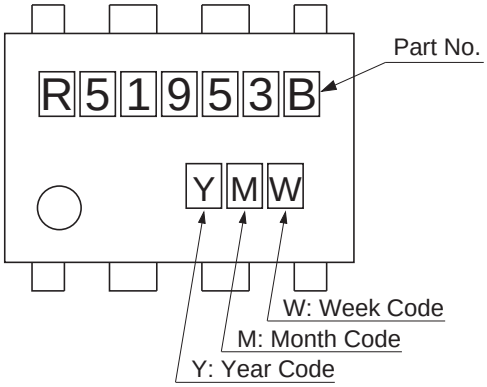


Y: Year Code
(the last digit of year)
M: Month Code
W: Week Code
C: Control Code



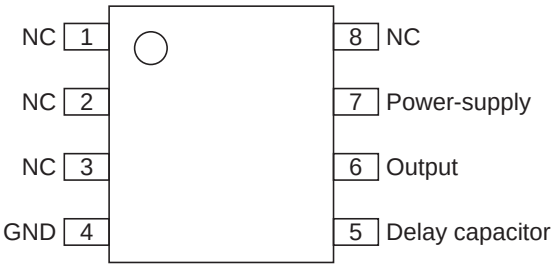
DIP-8





Pin Arrangement

RNA51953A, B

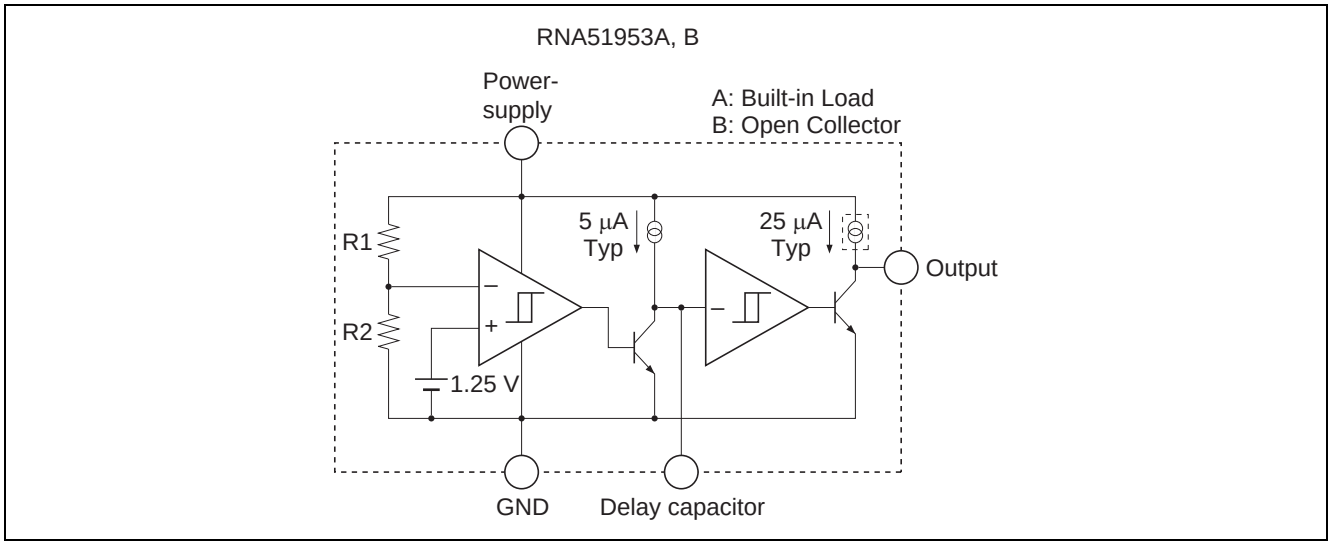


(Top view)

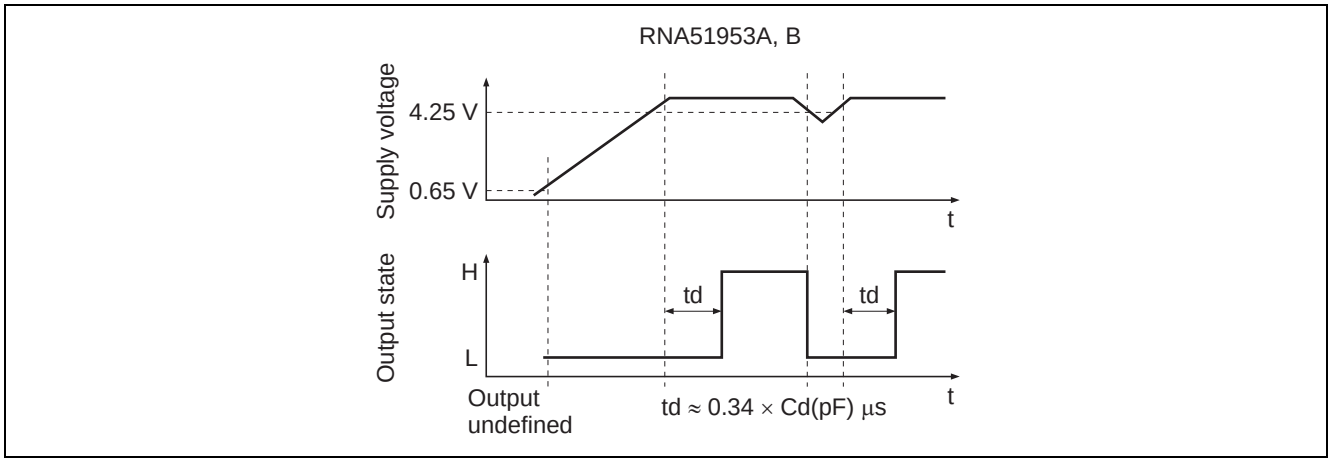
NC: No Connection

Outline: PRSP0008DE-C (SOP-8)
PRDP0008AF-B (DIP-8)

Block Diagram



Operating Waveform



Absolute Maximum Ratings

(Ta = 25°C, unless otherwise noted)

Item	Symbol	Ratings	Unit	Conditions	
Supply voltage	V_{CC}	18	V		
Output sink current	Isink	6	mA		
Output voltage	V_O	V_{CC}	V	Type A (output with constant current load)	
		18		Type B (open collector output)	
Power dissipation	Pd	400	mW	8-pin SOP (PRSP0008DE-C)	
		570		8-pin DIP (PRDP0008AF-B)	
Thermal derating	Kθ	4.4	mW/°C	8-pin SOP (PRSP0008DE-C)	Refer to the thermal derating curve.
		8.3		8-pin DIP (PRDP0008AF-B)	
Operating temperature	Topr	–40 to +85	°C		
Storage temperature	Tstg	–55 to +125	°C		

Electrical Characteristics

(Ta = 25°C, unless otherwise noted)

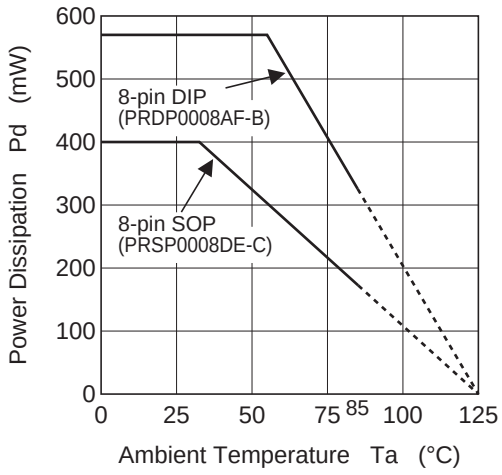
- "L" reset type

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Detecting voltage	V_S	4.05	4.25	4.45	V	
Hysteresis voltage	ΔV_S	30	50	80	mV	
Detecting voltage temperature coefficient	$V_S/\Delta T$	—	0.01	—	%/°C	
Circuit current	I_{CC}	—	450	680	μA	Type A, V_{CC} = 5V
		—	420	630		Type B, V_{CC} = 5V
Delay time	t_{pd}	1.6	3.4	7.0	ms	Cd = 0.01μF *
Constant current	Ipd	–8	–5	–3	μA	V_{CC} = 5V
Output saturation voltage	Vsat	—	0.2	0.4	V	V_{CC} = 4V, Isink = 4mA
Threshold operating voltage	V_{OPL}	—	0.67	0.8	V	R_L = 2.2kΩ, Vsat ≤ 0.4V
		—	0.55	0.7		R_L = 100kΩ, Vsat ≤ 0.4V
Output leakage current	I_{OH}	—	—	30	nA	Type B
Output load current	I_{OC}	–40	–25	–17	μA	Type A, V_{CC} = 5V, V_O = 1/2 × V_{CC}
Output high voltage	V_{OH}	V_{CC}–0.2	V_{CC}–0.06	—	V	Type A

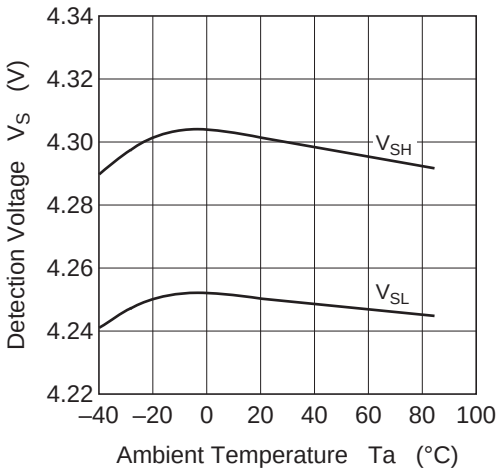
Note: Please set the desired delay time by attaching capacitor of the range between 4700 pF and 10 μF.

Typical Characteristics

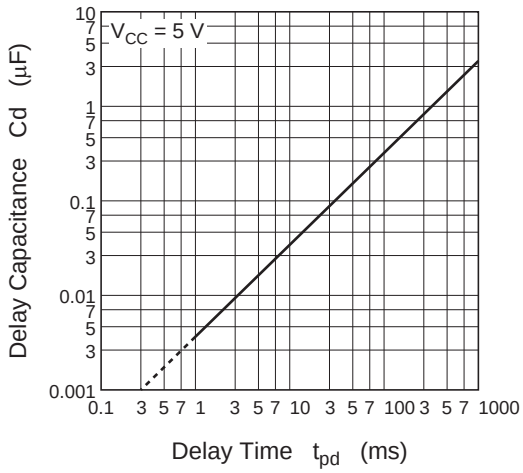
Thermal Derating



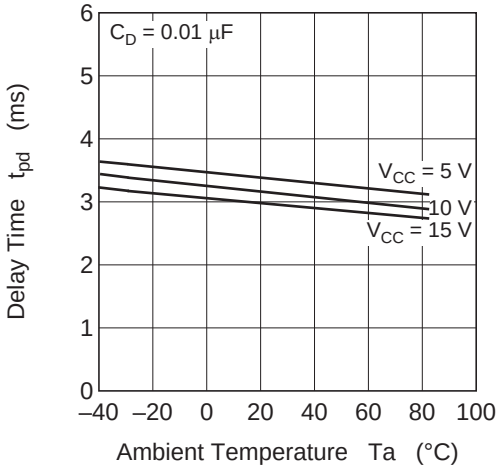
Detection Voltage vs. Ambient Temperature



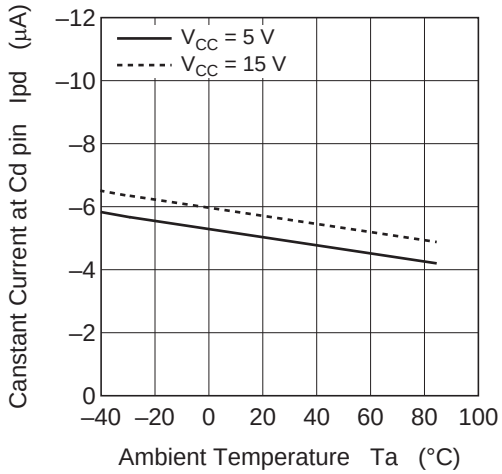
Delay Capacitance vs. Delay Time



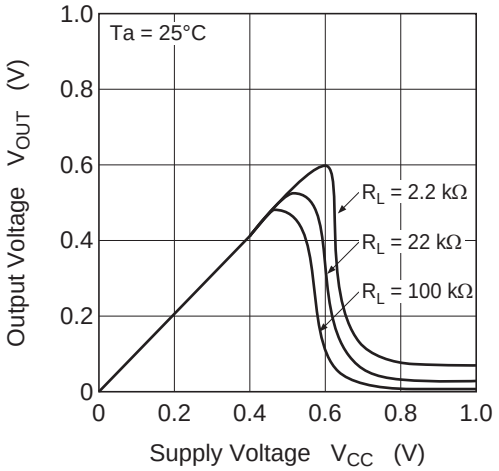
Delay Time vs. Ambient Temperature



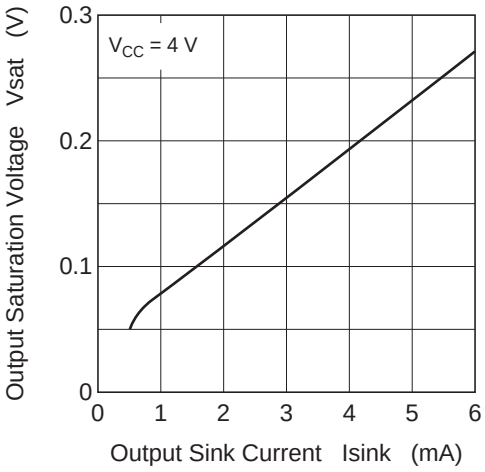
Canstant Current at Cd pin vs. Ambient Temperature



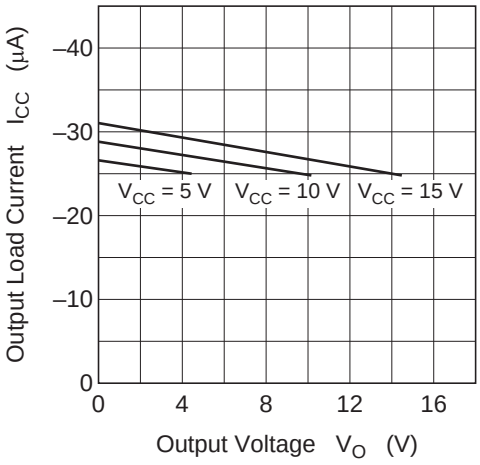
Threshold Operating Voltage



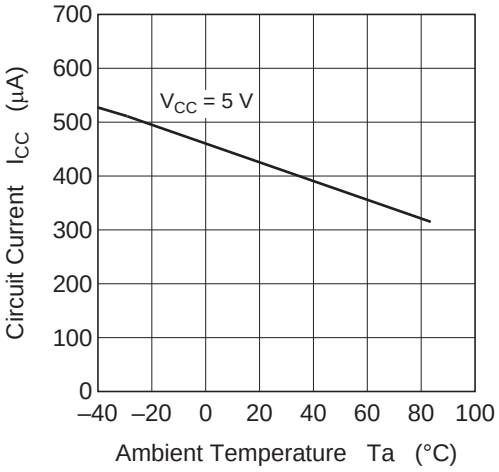
Output Saturation Voltage vs. Output Sink Current



Output Load Current vs. Output Voltage
(RNA51953A)



Circuit Current vs. Ambient Temperature
(RNA51953B)



Example of Application Circuit

Reset Circuit of RNA51953

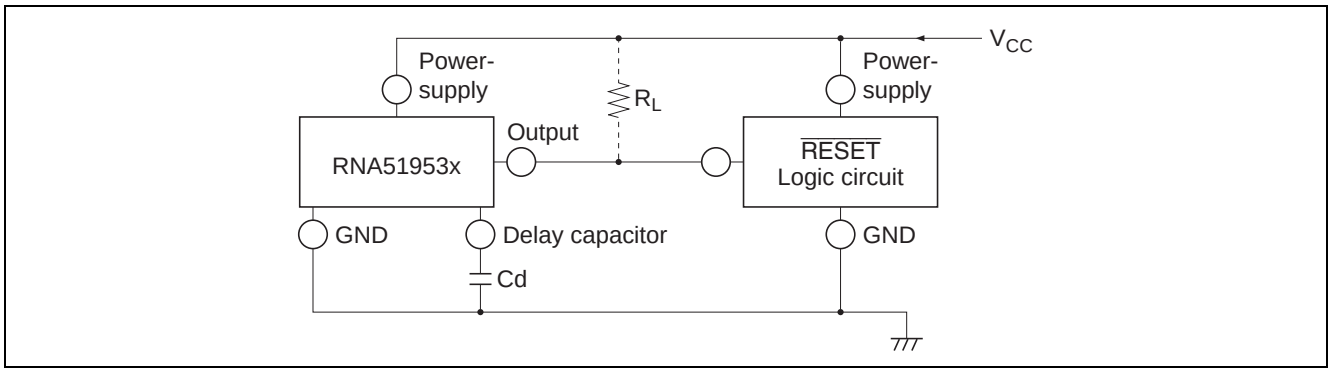


Figure 1 Reset Circuit of RNA51953

Notes: 1. When the voltage is anything except 4.25 V, RNA51957 and RNA51958 are used. In this case, the detecting supply voltage is $1.25 \times (R_1 + R_2)/R_2$ (V) approximately.
The detecting supply voltage can be set between 2 V and 15 V.
2. The delay time is about $0.34 \times$ Cd (pF) µs.
3. If the RNA51953 and the logic circuit share a common power source, type A (built-in load type) can be used whether a pull-up resistor is included in the logic circuit or not.
4. The logic circuit preferably should not have a pull-down resistor, but if one is present, add load resistor R_L to overcome the pull-down resistor.
5. When the reset terminal in the logic circuit is of the low reset type, RNA51953 and RNA51957 are used and when the terminal is of the high reset type, RNA51958 are used.
6. When a negative supply voltage is used, the supply voltage side of RNA51953 and the GND side are connected to negative supply voltage respectively.

Case of Using Reset Signal except Supply Voltage in the RNA51953

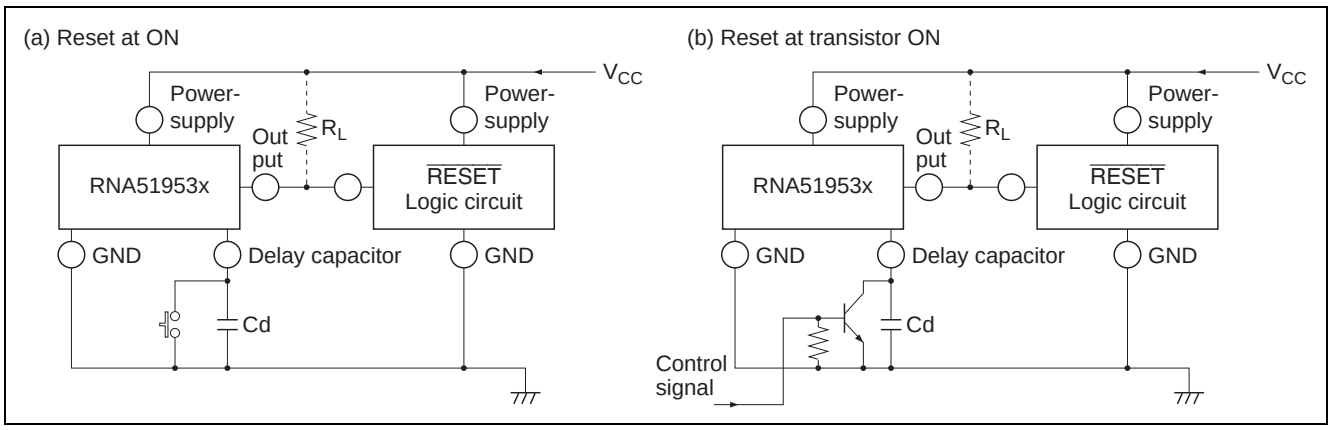


Figure 2 Case of Using Reset Signal except Supply Voltage in the RNA51953

Notice for use

About the Power Supply Line

1. About bypass capacitor
   Because the ripple and the spike of the high frequency noise and the low frequency are superimposed to the power supply line, it is necessary to remove these.
   Therefore, please install C_1 and C_2 for the low frequency and for the high frequency between the power supply line and the GND line as shown in following figure 3.

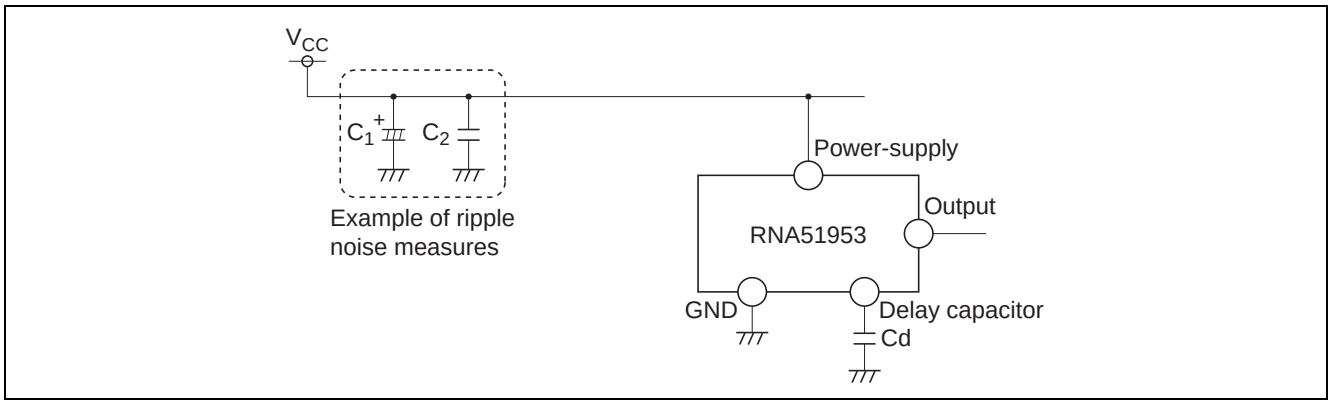


Figure 3 Example of Ripple Noise Measures

Setting of Delay Capacity

Please use capacitor Cd for the delay within the range of 10 μF or less.

When a value that is bigger than this is set, the problem such as following (1), (2), and (3) becomes remarkable.

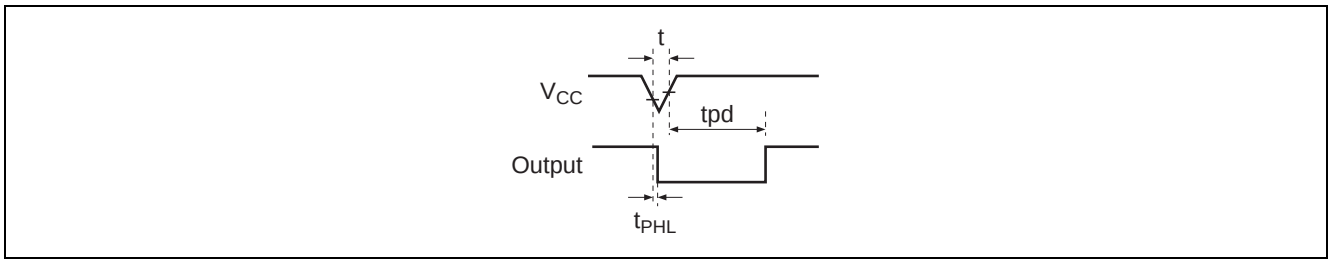


Figure 4 Time Chart at Momentary Voltage-Decrease

(1) The difference at delay time becomes remarkable.
A long delay setting of tens of seconds is fundamentally possible. However, when set delay time is lengthened, the range of the difference relatively grows, too. When a set value is assumed to be 'tpd', the difference occurs in the range from 0.47 × tpd to 2.05 × tpd. For instance, 34 seconds can be calculated at 100 μF. However, it is likely to vary within the ranges of 16-70 seconds.

(2) Difficulty to react to a momentary voltage decrease.
For example, the reaction time t_{PHL} is 10 μs when delay capacitor Cd = 0.1 μF.
The momentary voltage-decrease that is longer than such t_{PHL} are occurs, the detection becomes possible. When the delay capacitance is enlarged, t_{PHL} also becomes long. For instance, it becomes about 100 to 200 μs in case of circuit constant C1 = 100 μF.
(Characteristic graph 1 is used and extrapolation in case of Cd = 100 μF.)
Therefore, it doesn't react to momentary voltage-decrease that is shorter than this.

(3) Original delay time is not obtained.
When the momentary voltage-decrease time 't' is equivalent to t_{PHL}, the discharge becomes insufficient and the charge starts at that state. This phenomenon occurs at large capacitance. And, original delay time tpd is not obtained.
Please refer to characteristic graph 2. (Delay time versus input pulse width)

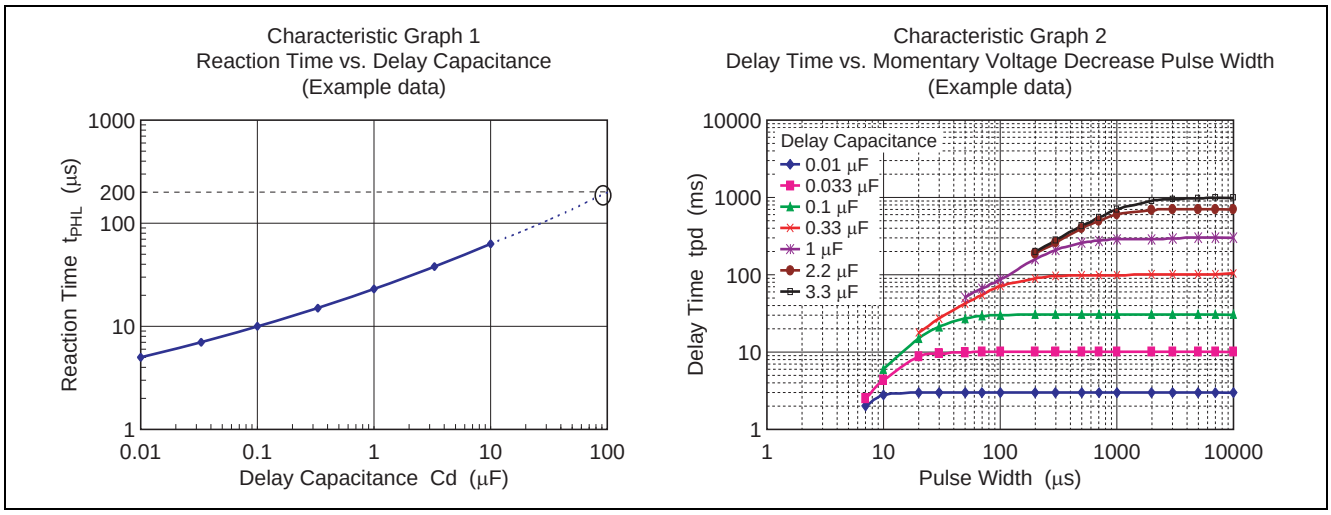


Figure 5 Characteristic Graph

Setting of Output Load Resistance (RNA51953B)

High level output voltage can be set without depending on the power-supply voltage because the output terminal is an open collector type. However, please guard the following notes.

1. Please set it in value (2 V to 17 V) within the range of the power-supply voltage recommendation.
   Moreover, please never impress the voltage of maximum ratings 18 V or more even momentarily either.
2. Please set output load resistance (pull-up resistance) R_L so that the output current (output inflow current I_L) at L level may become 4 mA or less. Moreover, please never exceed absolute maximum rating (6 mA).

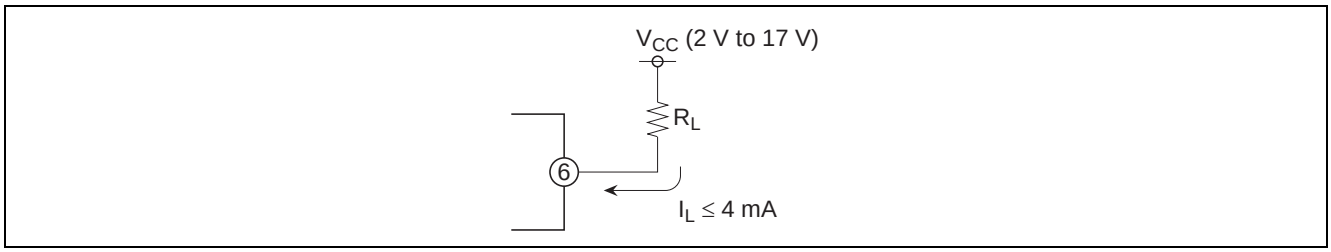


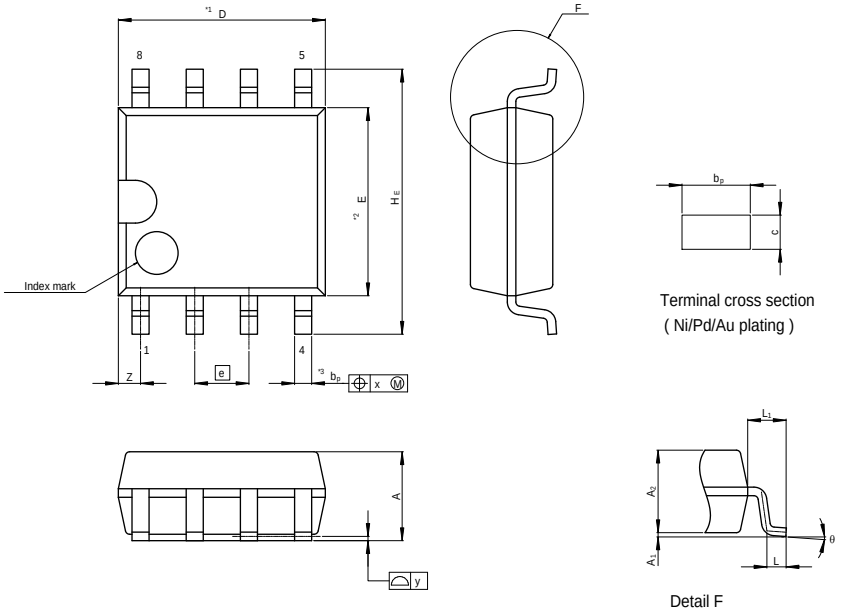
Figure 6 Output Load Resistance R_L

Others

1. Notes when IC is handled are published in our reliability handbook, and please refer it.
   The reliability handbook can be downloaded from our homepage (following URL).
   http://www.renesas.com/products/common_info/reliability/reliability_root.jsp
2. Additionally, please inquire of our company when there is an uncertain point on use.

Package Dimensions

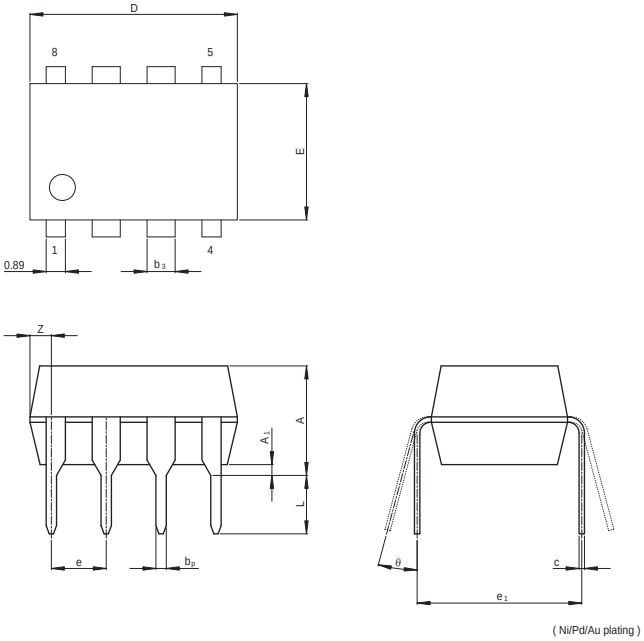
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP8-4.4x4.85-1.27	PRSP0008DE-C	—	0.1g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.65	4.85	5.05
E	4.2	4.4	4.6
A_2	—	1.85	—
A_1	0.00	0.1	0.20
A	—	—	2.03
b_p	0.34	0.4	0.46
b_1	—	—	—
c	0.15	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	5.7	6.2	6.5
e	1.12	1.27	1.42
x	—	—	0.12
y	—	—	0.10
Z	—	—	0.75
L	0.25	0.45	0.65
L_1	—	0.90	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP8-6.3x9.6-2.54	PRDP0008AF-B	DP-8FV	0.54g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	—	7.62	—
D	—	9.60	10.6
E	—	6.30	7.4
A	—	—	5.06
A_1	0.5	—	—
b_p	0.40	0.48	0.56
b_3	—	1.30	—
c	0.19	0.25	0.31
θ	0°	—	15°
e	2.29	2.54	2.79
Z	—	—	1.27
L	2.54	—	—

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